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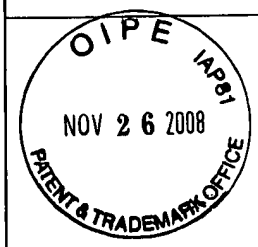
PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
JRL-550-534



Application Number	Filed
10/802,032	March 17, 2004
First Named Inventor: NIGHTINGALE	
Art Unit: 2123	Examiner: Janakiraman, Nithya

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ Applicant/Inventor

☐ Assignee of record of the entire interest. See 37 C.F.R. § 3.71. Statement under 37 C.F.R. § 3.73(b) is enclosed. (Form PTO/SB/96)

☒ Attorney or agent of record 33,149 (Reg. No.)

☐ Attorney or agent acting under 37CFR 1.34.
Registration number if acting under 37 C.F.R. § 1,34 _____

Signature

John R. Lastova
Typed or printed name

703-816-4025
Requester's telephone number

November 26, 2008
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.*

☒ *Total of 1 form/s are submitted.

If you need assistance in completing the form, call 1-800-PTO-9199 and selection option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

NIGHTINGALE, A. et al.

Atty. Ref.: 550-534; Confirmation No. 8029

Appl. No. 10/802,032

TC/A.U. 2123

Filed: March 17, 2004

Examiner: Janakiraman, Nithya

For: DATA PROCESSING APPARATUS SIMULATION

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November 26, 2008

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Commissioner for Patents
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Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Claims 1-26 stand rejected as failing to comply with the written description requirement. All claims 1-46 stand rejected for obviousness based on Fischer and Thekkath. These rejections are respectfully traversed.

Clear Error One: The Specification Supports "Machine-Readable"

The Examiner objects to the amendment in claims 1 and 12, i.e., "generating machine-readable revised timing information," contending that the term "machine-readable" is not supported by the description. But page 10, lines 6-12 of the specification explain how the "timing model generates revised or adjusted timing information ... As explained in more detail below, these signals in conjunction with signals from other timing models are used by the bus model 90 to determine which logic unit will gain access to the bus during any particular simulated clock cycle...."

The bus model 90 is part of the software simulation environment described at page 9, lines 1-19 and illustrated in Figure 2. The simulation model is implemented on a computer,

which is a machine. Therefore, the bus model 90 is also machine-implemented. Because the revised timing information is used by the bus model 90, the revised timing information is machine-readable.

Clearly, a person of ordinary skill in the art, reading the specification and viewing the figures, would conclude that the inventors in this application were in possession of the claimed feature "generating machine-readable revised timing information" at the time that this application was filed. Literal or explicit support for the term "machine-readable" is not required. See, e.g., *In re Kaslow*, 707 F.2d 1366 (Fed. Cir. 1983).

Clear Error Two: Neither Fischer Nor Thekkath Discloses A Method Of or An Apparatus For Simulating The Operation Of A Data Processing Apparatus"

The Examiner admits that Fischer does not disclose a method of or an apparatus for simulating, but argues that column 5, lines 29-37 of Thekkath does. Applicant disagrees. These lines describe "a computer program product for use in designing, simulating, fabricating, or testing an integrated bus master device. The computer program product has a storage medium that has computer readable instructions embodied thereon, for causing a computer upon which the computer readable instructions are executed to describe the integrated bus master device such that it can be modified, simulated, fabricated or tested." Thus, Thekkath describes a computer program that when executed provides a description of the integrated bus master device so that a simulation can be performed. This is merely a simulation platform that allows a simulation to be performed. Thekkath does not disclose how any simulation is actually performed – only that it is possible to do a simulation. Therefore, the combination fails to teach simulation method in claims 1 and 12, the simulation apparatus in claim 29, and the simulation program in claim 46.

For other features of claim 1, the Examiner draws on features from columns 6-7 of Thekkath. But these columns describe a real apparatus (see col. 6, lines 26-42 and Figure 1), not

a simulation. Moreover, columns 6 to 7 have nothing to do with the simulation platform described at column 5, since these columns describe separate embodiments.

Clear Error Three: Fischer Does Not Disclose Generating Anticipated Timing Information By Assuming That The Data Transfer Will Occur With Exclusive Access To The Bus

The Examiner cites [0012] of Fischer as disclosing generating anticipated timing information by assuming that the data transfer will occur with exclusive access to the bus. But there is no teaching in [0012] where it is assumed that data transfer will occur with exclusive access to the bus. Thekkath does not disclose any timing information. Thus, neither Fischer nor Thekkath discloses generating anticipated timing information by assuming that the data transfer will occur with exclusive access to the bus.

Clear Error Four: Thekkath Does Not Disclose Determining Whether The Anticipated Timing Information Indicates That Two Or More Concurrent Data Transfers Would Occur On The Bus

The Examiner cites col. 5, lines 1-10 of Thekkath as disclosing "detecting what would be the capability of the bus." But these lines do not disclose detecting a bus capability; instead, they state that the "slave configuration logic stores a burst transaction capability corresponding to the slave device." The burst transaction capability is a capability of the slave device—not the bus. Column 5, lines 6-7 confirms this: "By configuring bursts sequences in accordance with the slave device's ability to accept bursts...." So Thekkath does not detect a capability of the bus.

But even if Thekkath did disclose detecting a capability of the bus, (which it does not), that would not disclose "determining whether the anticipated timing information indicates that two or more concurrent data transfers would occur on the bus." Detecting a capability of the bus is not the same as determining whether the anticipated timing information indicates that two or more concurrent data transfers would occur on the bus. Thekkath describes bus arbitration logic 104 at col. 7, lines 1-31 as simply determining whether transaction requests have been received

from initiating devices, and granting or refusing requests according to an arbitration algorithm. There is no description of analyzing any anticipated timing information associated with the requests to determine whether two or more concurrent data transfers would occur on the bus.

Clear Error Five: Fischer And Thekkath Do Not Disclose Generating Machine-Readable Revised Timing Information For Those Data Transfers

In paragraph 23 of the final action, the Examiner states that "Fischer teaches that continuous revisions take place to adjust for the transaction interference, or errors, of Thekkath in paragraph 0012 [of Fischer], 'Each slave node clock is continuously corrected compared with the master node clock to smooth slave clock error to an average of zero compared with the master clock...'"

However, the continuous slave node clock correction of Fischer is not a correction of timing information. The slave node clock is a clock signal that controls operation of the slave device. The slave node clock is not timing information for concurrent data transfers, as recited in the claims. At no point does paragraph 0012 of Fischer describe revising anticipated timing information for two or more concurrent data transfers.

Clear Error Six: Fischer and Thekkath Cannot Be Sensibly Combined

Fischer and Thekkath are in different arts. Thekkath is in the field of computer system bus architectures (col. 1, lines 25-26) and teaches a computer system comprising a system bus and various processing circuits connected to the bus (see Figure 1). Each processing circuit is housed in a common computer housing. The various processing circuits 104-120 operate under control of the central processing unit 102. In contrast, Fischer is in the field of communications networks. The "nodes" of the network in Fischer are separate devices within a communications network, such as computers, printers, scanners, telephones, televisions, cameras etc (see [0106]

and Figures 1a-1c of Fischer). There is no one central processing unit that operates the various devices in the network—each device has its own control capability.

There is no reasonable basis for a skilled person to use a technique for arbitrating requests for transfers on an internal system bus in communications between separate nodes externally connected by a network. Fischer's communications network will typically have many thousands of terminals (see the many houses in Figure 1c of Fischer) with fiber optic cables being used so that multiple data transfers can be carried across the network at the same time. The Examiner admits that Fischer does not compensate for two or more concurrent transactions. The reason Fischer does not do such compensation is that preventing two or more concurrent transactions would result in thousands of people being cut off from the network every time a single person uses the network, which would not be sensible. Given that this kind of exclusive access to the network is clearly undesirable in a network such as Fischer's, the skilled person would not introduce a bus arbiter (as described in Thekkath) into the network in order to enforce exclusive network access.

Respectfully submitted,
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